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10/813,834	03/31/2004	Keiichiro Tounai	NEC A433	6044

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EXAMINER	
PARK, EDWARD	

ART UNIT	PAPER NUMBER
2624	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/813,834	TOUNAI, KEIICHIRO	
	Examiner	Art Unit	
	EDWARD PARK	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/20/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 5/19/09, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Samir A. Ahmed/

Supervisory Patent Examiner, Art Unit 2624

2. Claims 1-26 are currently pending.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-7, 15-20, 21, 22, 25, 26 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. The Federal Circuit[1], relying upon Supreme Court precedent[2], has indicated that a statutory "process" under 35 U.S.C. 101 must (1) be tied to a particular machine or apparatus, or (2) transform a particular article to a different state or thing. This is referred to as the "machine or transformation test", whereby the recitation of a particular machine or transformation of an article must impose meaningful limits on the claim's scope to impart patent-eligibility (See *Benson*, 409 U.S. at 71-72), and the involvement of the machine or transformation in the claimed process must not merely be insignificant extra-solution activity (See *Flook*, 437 U.S. at 590"). While the instant claim(s) recite a series of steps or acts to be performed, the claim(s) neither transform an article nor are positively tied to a particular machine that accomplishes the claimed method steps, and therefore do not qualify as a statutory process. That is, the method includes steps of applying, dividing, determining, simulating, checking, etc. is of sufficient breadth that it would be reasonably interpreted as a series of steps completely performed mentally, verbally, or without a machine. The cited claims do not positively recite

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[1] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

[2] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

any structure within the body of the claim which ties the claim to a statutory category. Furthermore, the examiner suggests that the structure needs to tie in the basic inventive concept of the application to a statutory category. Structure that ties insignificant pre or post solution activity to a statutory category is not sufficient in overcoming the 101 issue. Additionally, the limitations do not claim data that represents a physical object or substance, the data representing the physical object is not present and therefore can not be modified by the process in a meaningful or significant manner, and no meaningful and significant external, non-data depiction of a physical object or substance is produced. Thus, the limitations do not satisfy the transformation test.

[1] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

[2] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 4, 5, 8, 11, 12, 15, 18, 19, 21-26** are rejected under 35 U.S.C. 102(b) as being anticipated by Tounai (US 6,174,633 B1).

Regarding **claim 1**, Tounai discloses a method of testing a mask pattern, comprising the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see col. 2, lines 24-34; correcting a photo-contiguous effect during manufacturing a semiconductor device including the steps of: designating a first region specified by a first mask pattern of a first level mask);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see fig. 4, col. 3, lines 30-40; interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66);

determining sampling points on an edge of said first pattern (see fig. 4, see col. 3, lines 39-50; computer 66 locates a first and a second corners 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24);

determining a test standard for each of said areas (see fig. 4, col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 2, lines 13-18, 34-40; correcting a photo-contiguous effect during manufacture of a semiconductor device); and

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (see col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see fig. 4, col. 3, lines 30-50; regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66; regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19).

Regarding **claim 4**, Tounai discloses pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (see fig. 5, col. 4, lines 13-55).

Regarding **claim 5**, Tounai discloses a contact area and an ambient area surrounding said contact area (see fig. 5, col. 4, lines 13-55).

Regarding **claim 8**, Tounai discloses a computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern (see fig. 3, lines 30-50), wherein said method is executed by said computer in accordance with said program including the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see col. 2, lines 24-34; correcting a photo-contiguous effect during manufacturing a semiconductor device including the steps of: designating a first region specified by a first mask pattern of a first level mask);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see fig. 4, col. 3, lines 30-40; interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66);

determining sampling points on an edge of said first pattern (see fig. 4, see col. 3, lines 39-50; computer 66 locates a first and a second corners 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66

establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24);

determining a test standard for each of said areas (see fig. 4, col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 2, lines 13-18, 34-40; correcting a photo-contiguous effect during manufacture of a semiconductor device); and checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (see col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see fig. 4, col. 3, lines 30-50; regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66; regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19).

Regarding **claim 11**, Tounai discloses pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a

third area including a contact area in which said contact makes contact with said wiring layer (see fig. 5, col. 4, lines 13-55).

Regarding **claim 12**, Tounai discloses a contact area and an ambient area surrounding said contact area (see fig. 5, col. 4, lines 13-55).

Regarding **claim 15**, Garza discloses a method of forming a mask having a desired mask pattern including the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see col. 2, lines 24-34; correcting a photo-contiguous effect during manufacturing a semiconductor device including the steps of: designating a first region specified by a first mask pattern of a first level mask);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see fig. 4, col. 3, lines 30-40; interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66);

determining sampling points on an edge of said first pattern (see fig. 4, see col. 3, lines 39-50; computer 66 locates a first and a second corners 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66

establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24);

determining a test standard for each of said areas (see fig. 4, col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 2, lines 13-18, 34-40; correcting a photo-contiguous effect during manufacture of a semiconductor device);

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs(see col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step); and

transferring said mask pattern onto a mask (see col. 3, lines 30-67, col. 4, lines 1-13), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see fig. 4, col. 3, lines 30-50; regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66; regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19).

Regarding **claim 18**, Tounai discloses pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (see fig. 5, col. 4, lines 13-55).

Regarding **claim 19**, Tounai discloses a contact area and an ambient area surrounding said contact area (see fig. 5, col. 4, lines 13-55).

Regarding **claim 21**, Tounai discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 22**, Tounai discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 23**, Tounai discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 24**, Tounai discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 25**, Tounai discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 26**, Tounai discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 3, lines 30-63).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 2, 3, 9, 10, 16, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tounai (US 6,174,633 B1) in view of Tsudaka (US 5,991,006).

Regarding **claims 2, 3**, Tounai discloses all elements as mentioned above in claim 1. Tounai does not teach N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Tsudaka, in the same field of endeavor, teaches N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another (see col. 2, lines 34-67; col. 3, lines 1-15; transferred image as being closest possible to the desired design pattern in the lithography process. More specifically, the method comprises the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred pattern image after the exposure by simulation; computing a distance between each evaluation point or each edge and a position corresponding to each evaluation point of the transferred image of the exposed pattern; and determining a corrected exposure pattern by inputting the distance to a specified evaluation function to correct

the position of each edge according to an output value of the evaluation function. The above method of the present invention further includes the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred energy intensity of the exposed pattern by simulation; determining a corrected exposure pattern by inputting the transferred energy intensity to a specified evaluation function to correct the position of each edge according to the output value of the evaluation function; plurality of a evaluation points are assigned to each of the edges obtained by dividing the visible outline of the object design pattern and computing the distance between each evaluation point and the position corresponding to each evaluation point on the exposed pattern image, and the distance between each of a plurality of the evaluation points and the exposure image on each edge can be computed); and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions (see col. 2, lines 34-67; col. 3, lines 1-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai to utilize multiple sampling points and standards as suggested by Tsudaka, in order to optimize a mask pattern for simulation and production by reducing time and processes in the correction of these irregular patterns (see col. 1, lines 20-48).

Regarding **claims 9, 10**, Tounai discloses all elements as mentioned above in claim 8. Tounai does not teach N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one

another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Tsudaka, in the same field of endeavor, teaches N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another (see col. 2, lines 34-67; col. 3, lines 1-15; transferred image as being closest possible to the desired design pattern in the lithography process. More specifically, the method comprises the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred pattern image after the exposure by simulation; computing a distance between each evaluation point or each edge and a position corresponding to each evaluation point of the transferred image of the exposed pattern; and determining a corrected exposure pattern by inputting the distance to a specified evaluation function to correct the position of each edge according to an output value of the evaluation function. The above method of the present invention further includes the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred energy intensity of the exposed pattern by simulation; determining a corrected exposure pattern by inputting the transferred energy intensity to a specified evaluation function to correct the position of each edge according to the output value of the evaluation function; plurality of a evaluation points are assigned to each of the edges obtained by dividing the visible outline of the object design pattern and computing the distance between each evaluation point and the position corresponding to each

evaluation point on the exposed pattern image, and the distance between each of a plurality of the evaluation points and the exposure image on each edge can be computed); and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions (see col. 2, lines 34-67; col. 3, lines 1-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai to utilize multiple sampling points and standards as suggested by Tsudaka, in order to optimize a mask pattern for simulation and production by reducing time and processes in the correction of these irregular patterns (see col. 1, lines 20-48).

Regarding **claims 16, 17**, Tounai discloses all elements as mentioned above in claim 15. Tounai does not teach N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Tsudaka, in the same field of endeavor, teaches N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another (see col. 2, lines 34-67; col. 3, lines 1-15; transferred image as being closest possible to the desired design pattern in the lithography process. More specifically, the method comprises the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred pattern image after the exposure by simulation;

computing a distance between each evaluation point or each edge and a position corresponding to each evaluation point of the transferred image of the exposed pattern; and determining a corrected exposure pattern by inputting the distance to a specified evaluation function to correct the position of each edge according to an output value of the evaluation function. The above method of the present invention further includes the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred energy intensity of the exposed pattern by simulation; determining a corrected exposure pattern by inputting the transferred energy intensity to a specified evaluation function to correct the position of each edge according to the output value of the evaluation function; plurality of a evaluation points are assigned to each of the edges obtained by dividing the visible outline of the object design pattern and computing the distance between each evaluation point and the position corresponding to each evaluation point on the exposed pattern image, and the distance between each of a plurality of the evaluation points and the exposure image on each edge can be computed); and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions (see col. 2, lines 34-67; col. 3, lines 1-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai to utilize multiple sampling points and standards as suggested by Tsudaka, in order to optimize a mask pattern for simulation and production by reducing time and processes in the correction of these irregular patterns (see col. 1, lines 20-48).

8. **Claims 6, 7, 13, 14, 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tounai (US 6,174,633 B1) in view of Miyazaki (US 6,665,858 B2).

Regarding **claims 6, 7**, Tounai discloses all elements as mentioned above in claim 1. Tounai does not teach pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern; and fifth area and an ambient area surrounding said fifth area.

Miyazaki, in the same field of endeavor, teaches pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (see col. 2, lines 1-17, col. 6, lines 64-67, col. 7, lines 1-21); and fifth area and an ambient area surrounding said fifth area (see col. 6, lines 64-67, col. 7, lines 1-21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai to utilize a wiring layer and multiple areas as suggested by Miyazaki, in order to ensure that the simulation and production of layers/patterns are accurately in compliance with design data (see col. 1, lines 53-63).

Regarding **claims 13, 14**, Tounai discloses all elements as mentioned above in claim 8. Tounai does not teach pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern; and fifth area and an ambient area surrounding said fifth area.

Miyazaki, in the same field of endeavor, teaches pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area

of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (see col. 2, lines 1-17, col. 6, lines 64-67, col. 7, lines 1-21); and fifth area and an ambient area surrounding said fifth area (see col. 6, lines 64-67, col. 7, lines 1-21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai to utilize a wiring layer and multiple areas as suggested by Miyazaki, in order to ensure that the simulation and production of layers/patterns are accurately in compliance with design data (see col. 1, lines 53-63).

Regarding **claim 20**, Tounai discloses all elements as mentioned above in claim 15. Tounai does not teach pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Miyazaki, in the same field of endeavor, teaches pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (see col. 2, lines 1-17, col. 6, lines 64-67, col. 7, lines 1-21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai to utilize a wiring layer and multiple areas as suggested by Miyazaki, in order to ensure that the simulation and production of layers/patterns are accurately in compliance with design data (see col. 1, lines 53-63).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD PARK whose telephone number is (571)270-1576. The examiner can normally be reached on M-F 10:30 - 20:00, (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Samir Ahmed can be reached on (571) 272-7413. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Edward Park
Examiner
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